

FIG 1

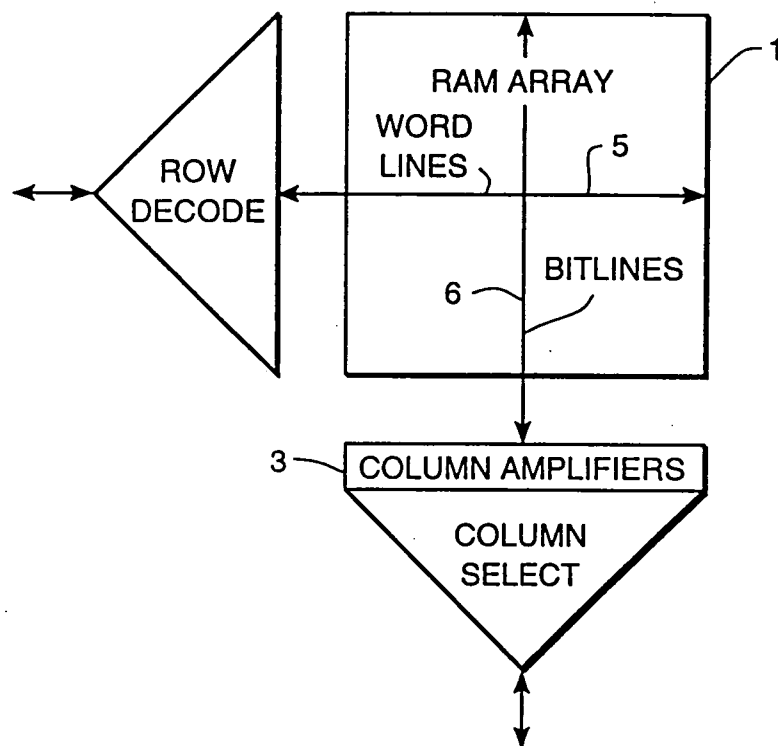


FIG. 2

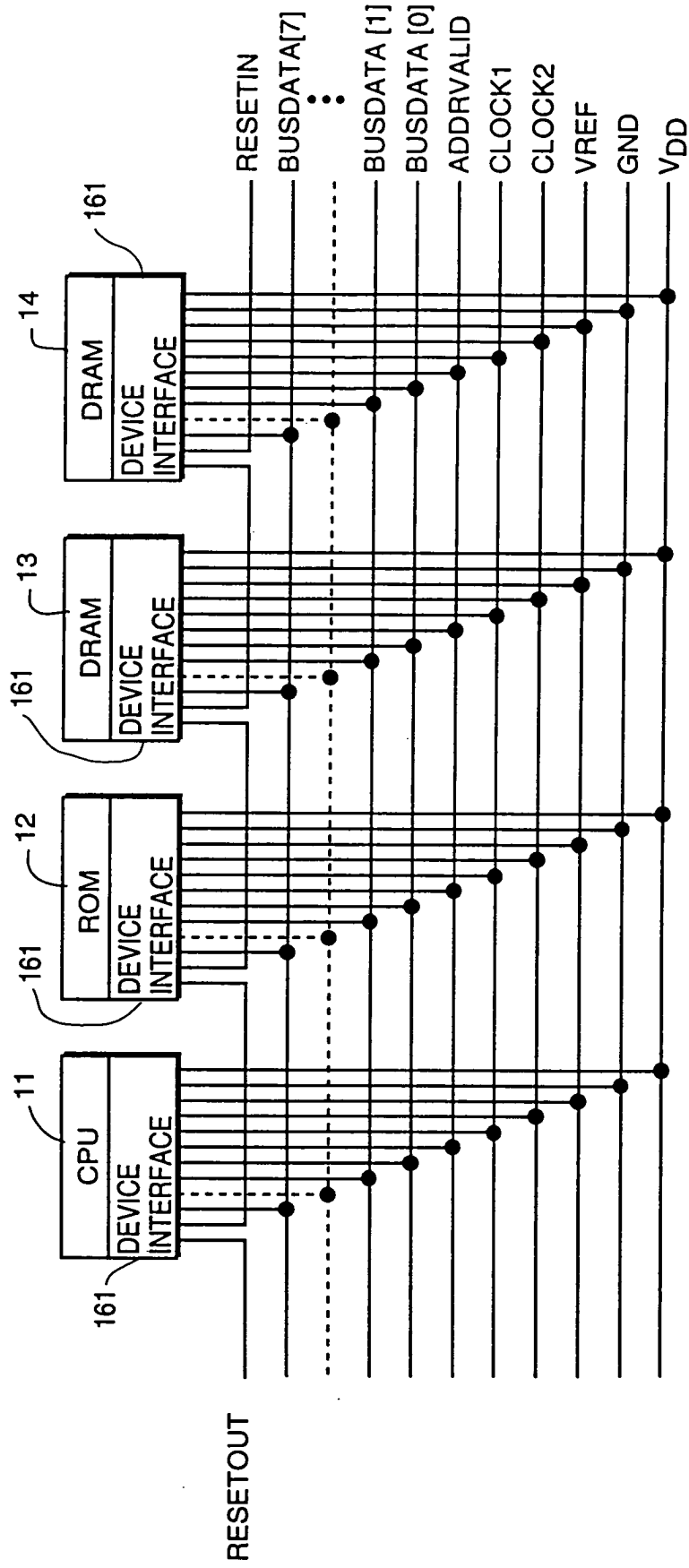
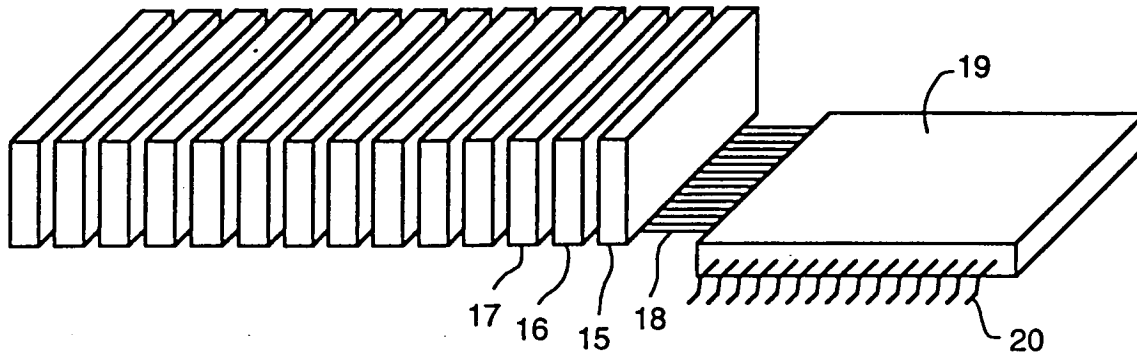


FIG 3



REGULAR ACCESS

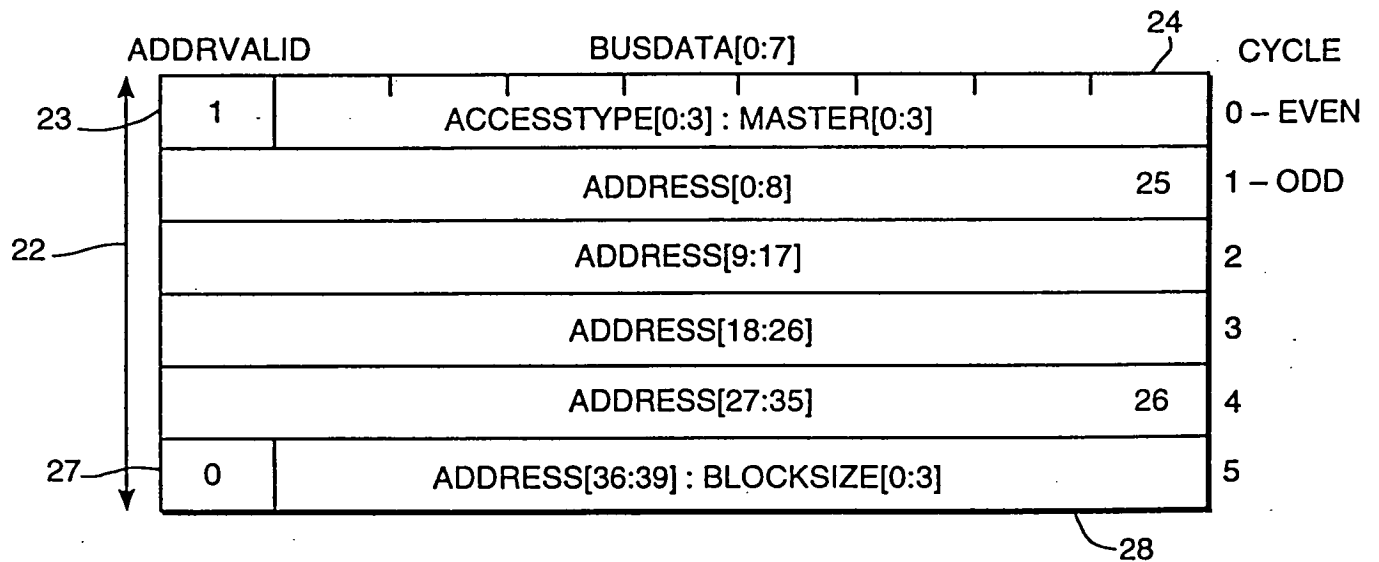


FIG 4

REJECT (NACK) CONTROL PACKET

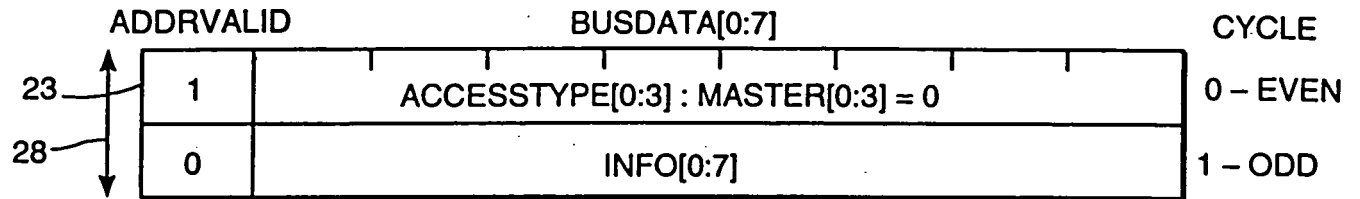


FIG 5

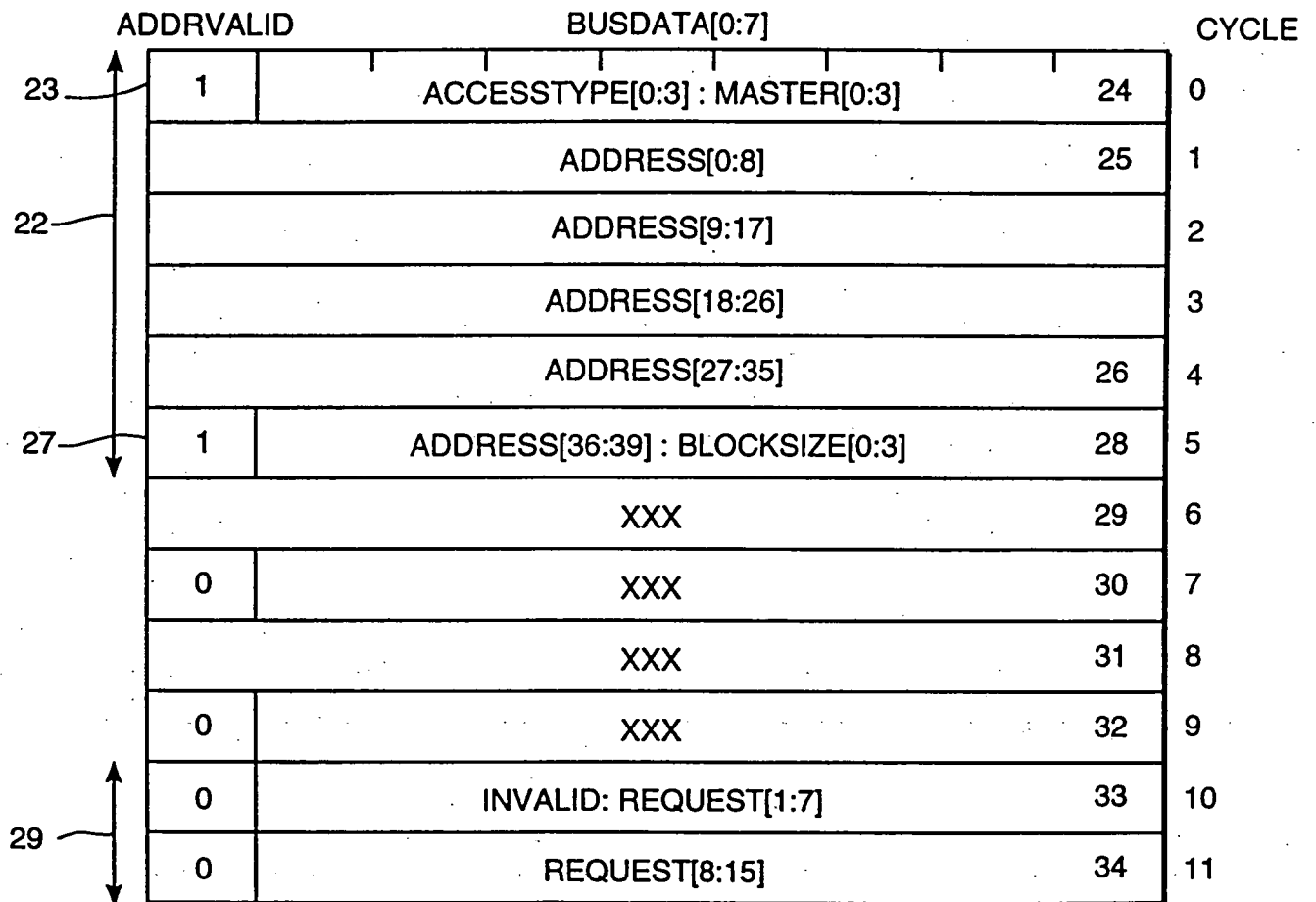
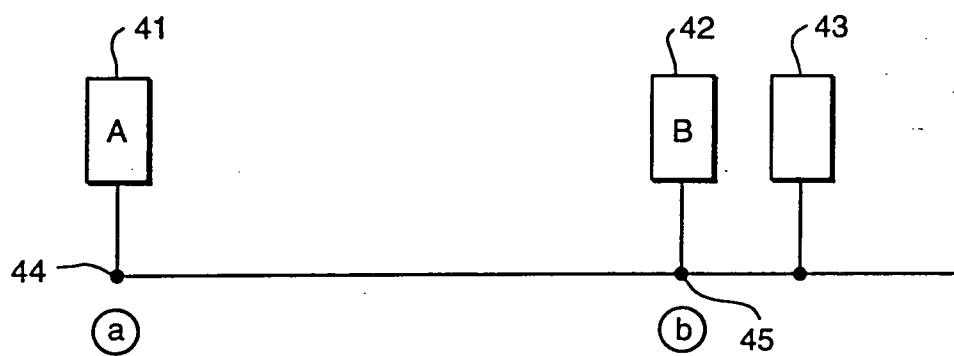


FIG 6



FIG_7A

LOGICAL
VOLTAGE
VALUE



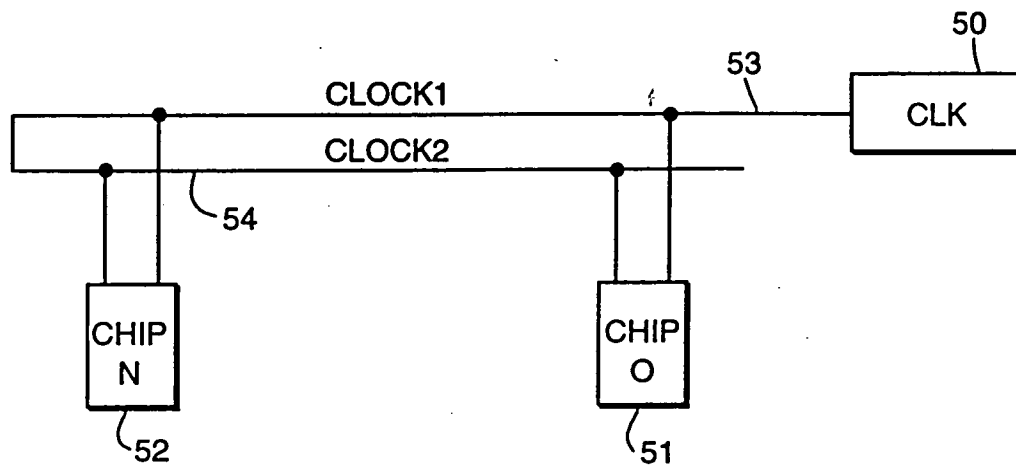


FIG 8A

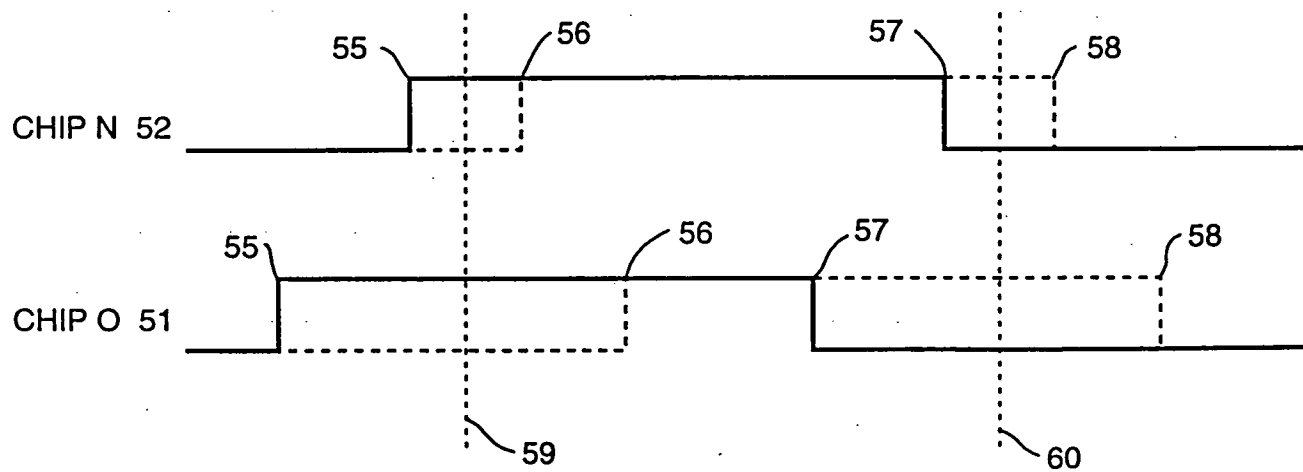
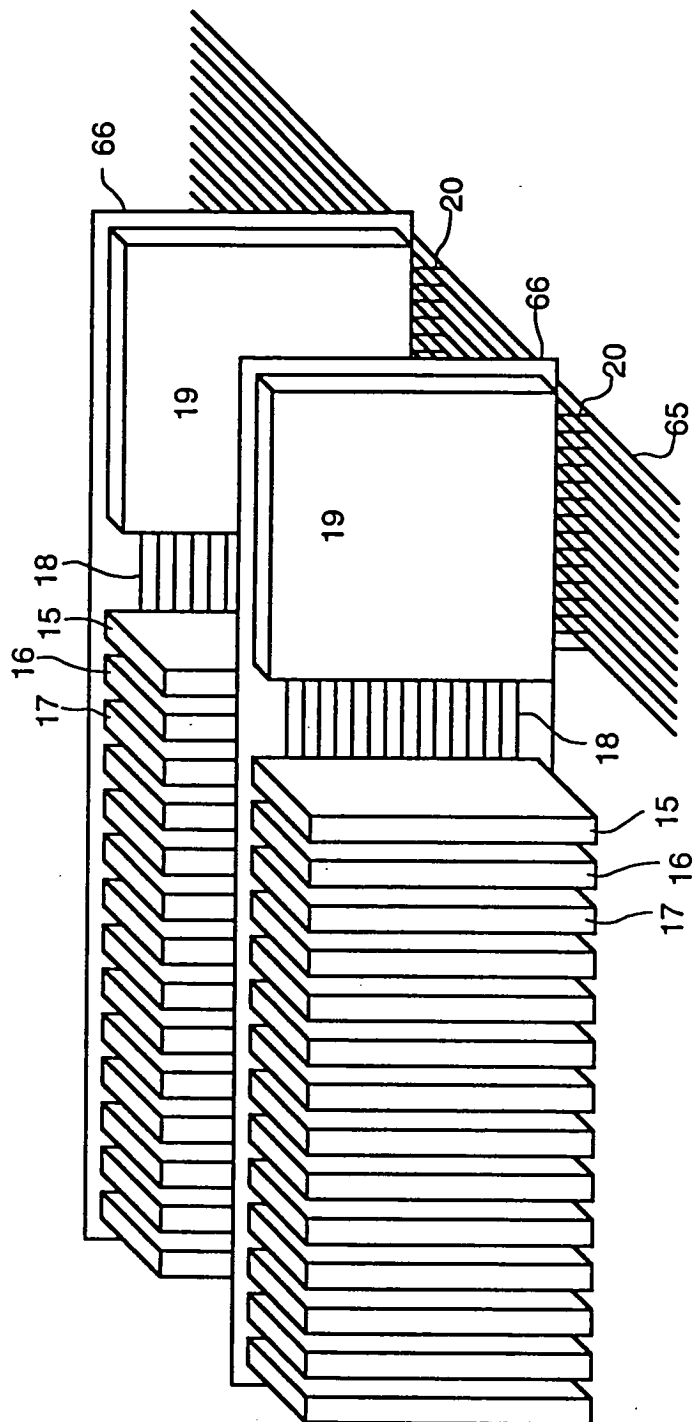


FIG 8B

FEIFE



THE

FIG 11

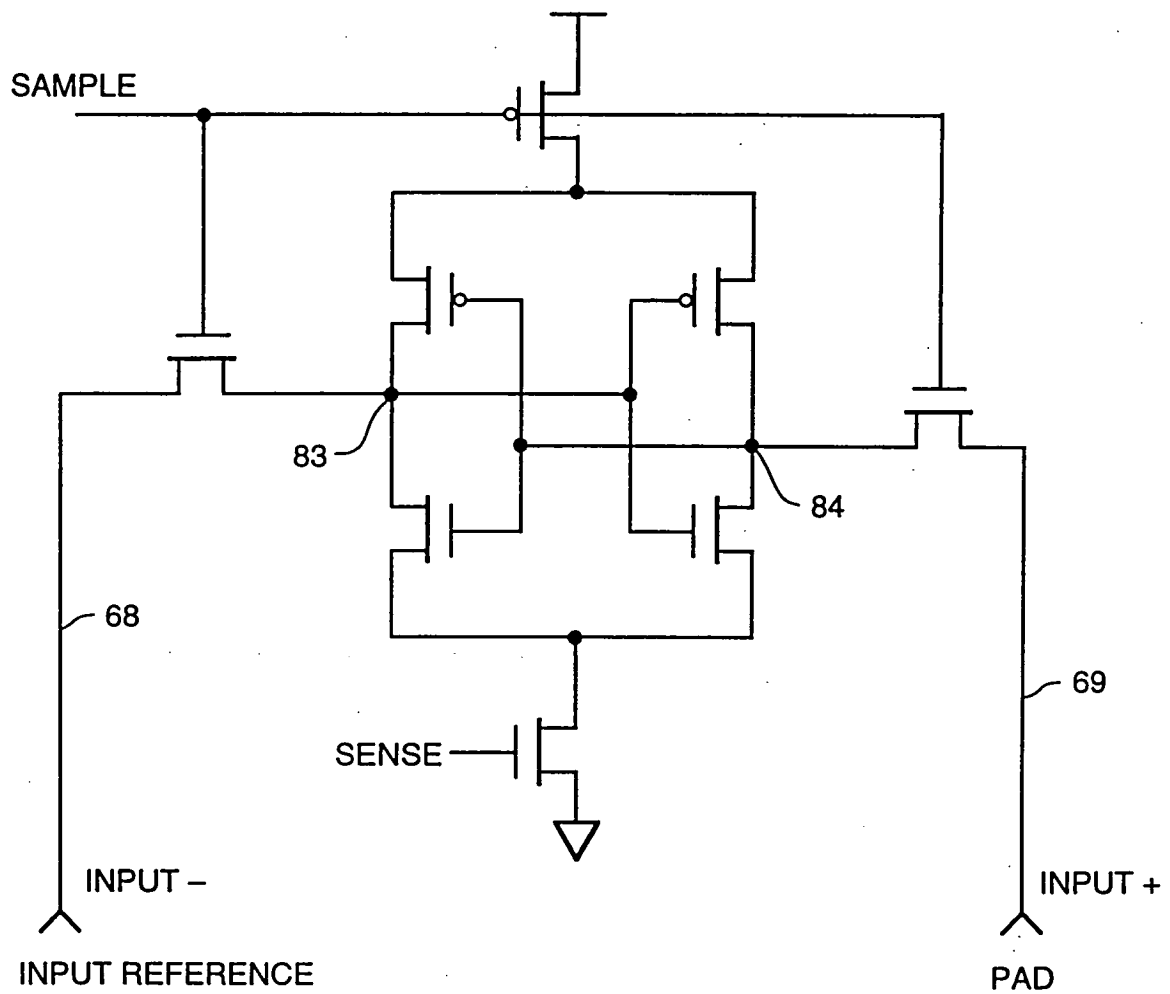


FIG. 12

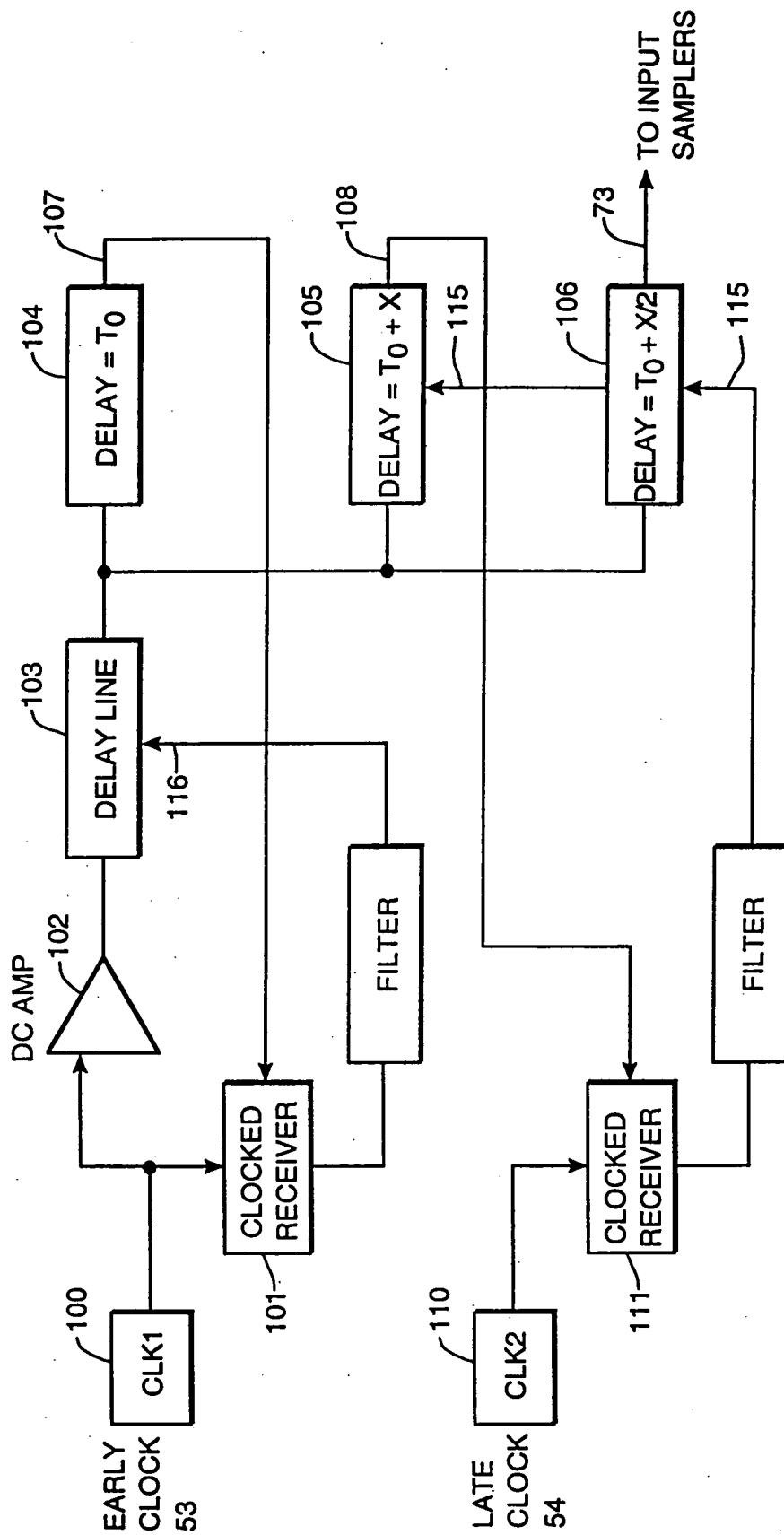
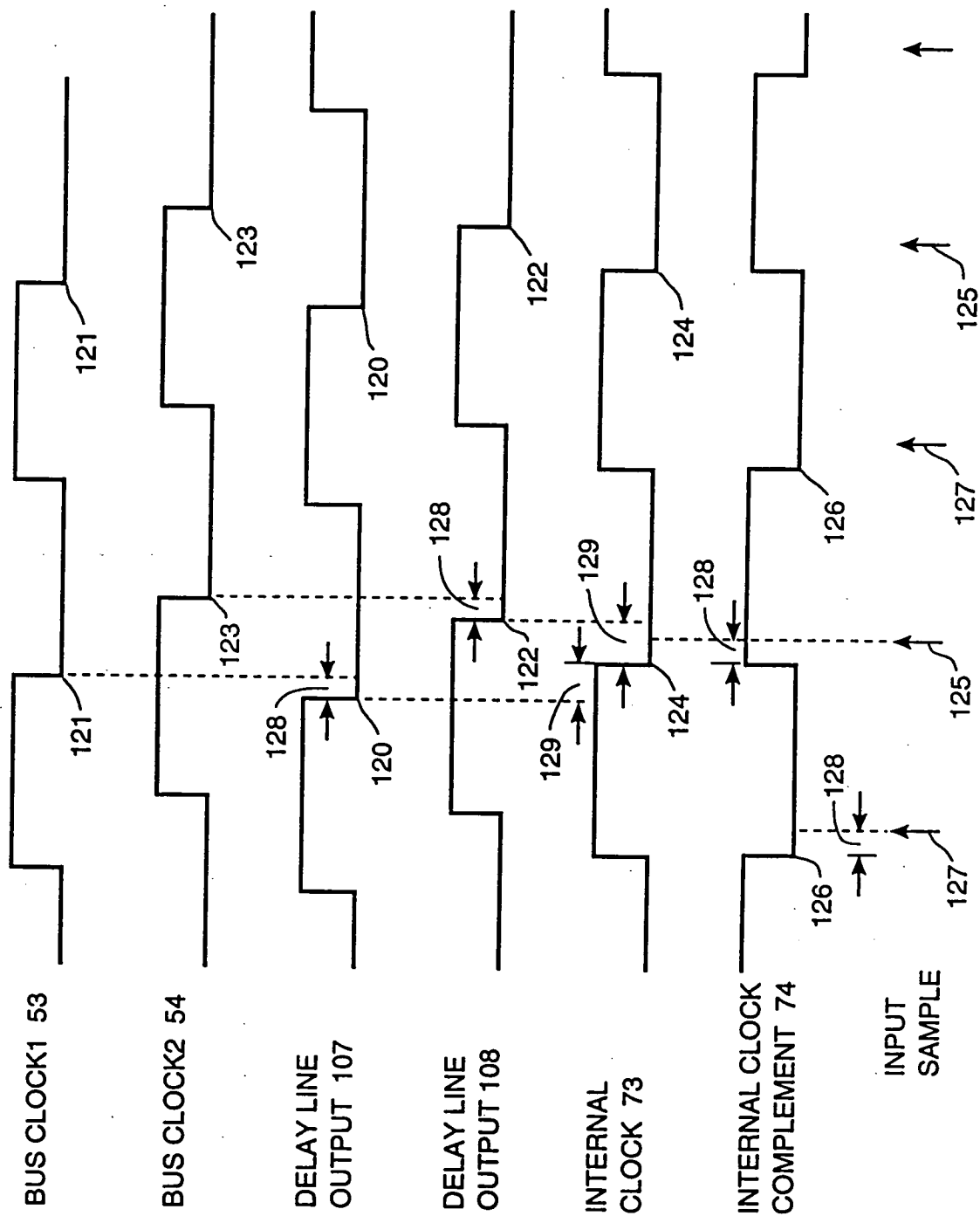


FIG 13



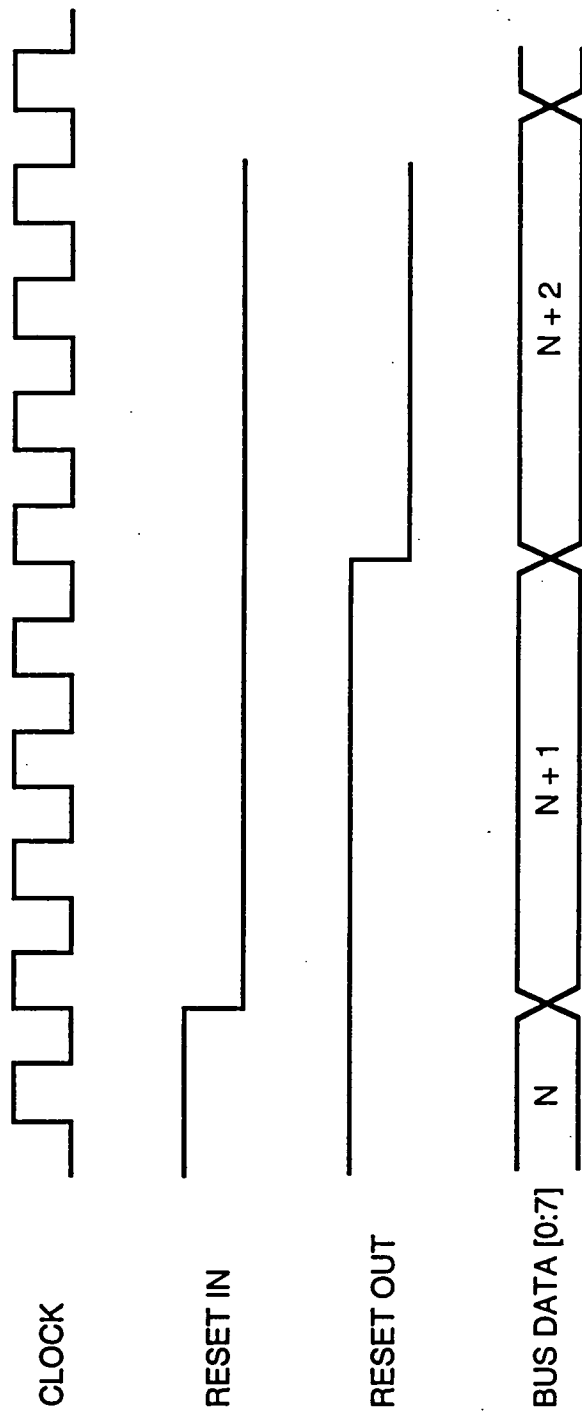
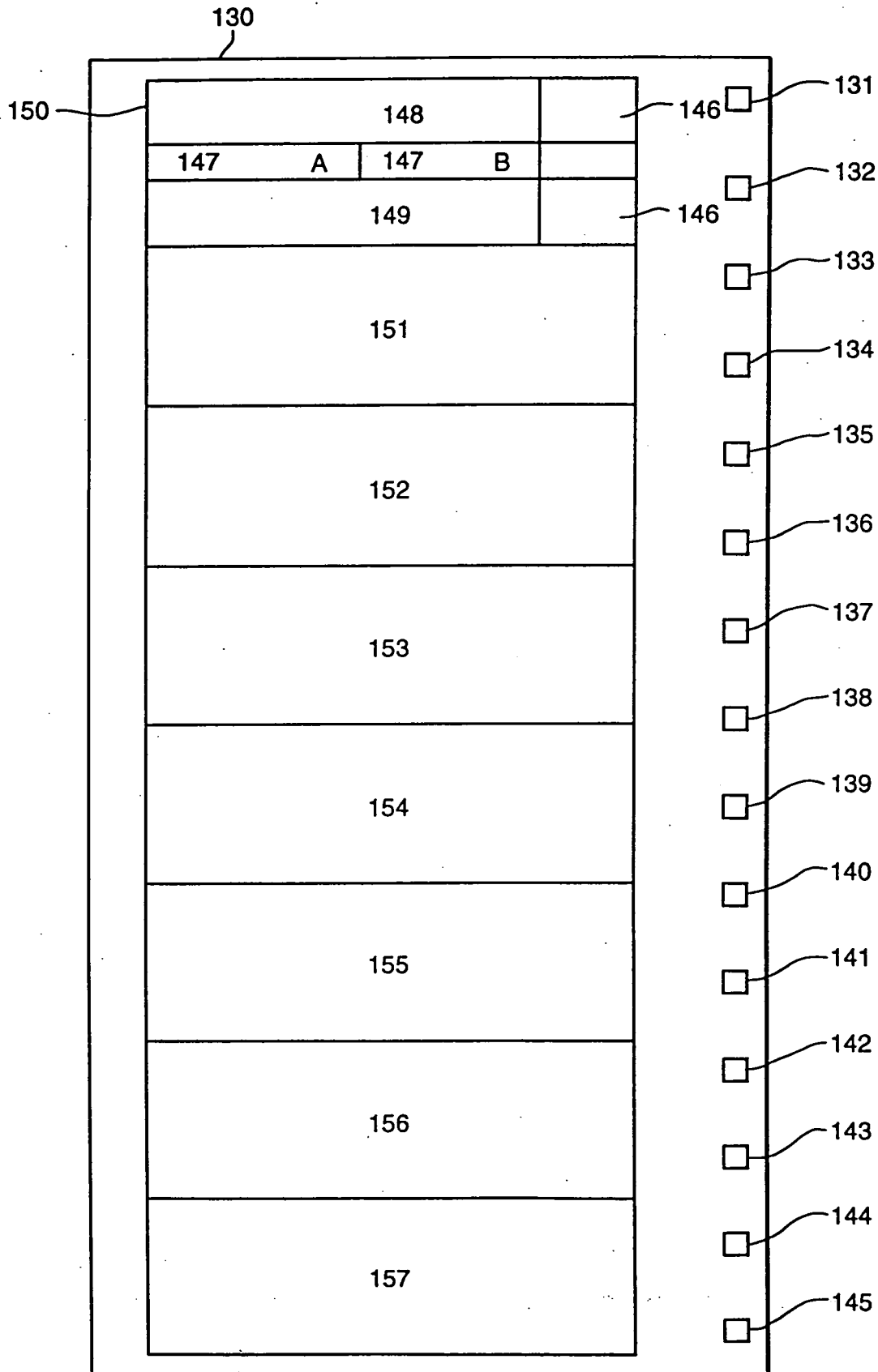


FIG 15



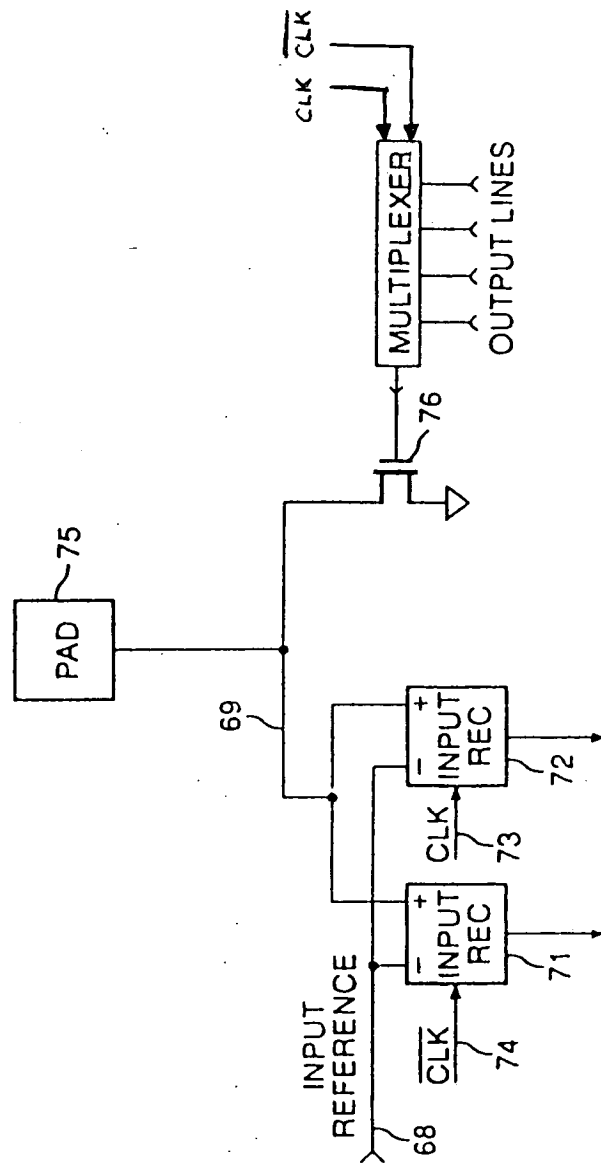
[illegible]

FIG. 10

Block diagram of a differential signal processing circuit. The circuit includes an input signal line (68) that splits into two paths. The first path passes through a buffer (76) and a multiplexer. The second path passes through a differential pair of input registers (71, 72) and a multiplexer. The multiplexer selects between the two paths based on a clock signal (CLK). The output is connected to a PAD (75).

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